Amendments to the Claims

This listing of the Claims will replace all prior versions and listings of the claims in this patent application.

Listing of the Claims

1. (currently amended) ~~An integrated~~ A circuit component ~~chip~~ comprising:

a semiconductor substrate ~~having semiconductor devices and interconnection lines formed thereover~~;

a transistor in and on said semiconductor substrate;

a power bus over said semiconductor substrate;

a ground bus over said semiconductor substrate;

~~a passivation layer overlying said substrate;~~

a ~~discrete~~ capacitor ~~mounted above~~ over said semiconductor substrate; ~~passivation layer; and~~

~~one or more wirebonds electrically connected to said discrete capacitor.~~

a first solder connection connecting said capacitor to said power bus; and

a second solder connection connecting said capacitor to said ground bus.

2. (currently amended) The ~~integrated~~ circuit component according to claim 1 further comprising a metallization structure over said semiconductor substrate, and a passivation layer over said metallization structure, wherein said power and ground buses are over

said passivation layer. ~~discrete capacitor is connected to said one or more wirebonds through said interconnection lines.~~

3. (currently amended) The ~~integrated~~ circuit component according to claim 1 further comprising:

a contact pad over said semiconductor substrate;

a passivation layer over said semiconductor substrate, an opening in said passivation layer exposing said contact pad; and

a wirebond on said contact pad. ~~wherein said one or more wirebonds connect to a contact pad exposed through openings in said passivation layer.~~

4. (withdrawn ~~and~~ -- currently amended) The ~~integrated~~ circuit component according to claim 1 further comprising a polymer layer over said semiconductor substrate, wherein said power bus is on said polymer layer. ~~wherein said capacitor connects to a contact pad formed in openings in said passivation layer.~~

5. (currently amended) The ~~integrated~~ circuit component according to claim 1 further comprising:

a first contact pad over said semiconductor substrate;

a passivation layer over said semiconductor substrate, an opening in said passivation layer exposing said first contact pad;

a second contact pad on said first contact pad; and

a wirebond on said second contact pad. ~~a metal line system overlying said passivation layer.~~

6. (currently amended) The ~~integrated~~ circuit component according to claim 1 ~~5~~ further comprising:

a contact pad over said semiconductor substrate; and

a wirebond on said contact pad, wherein said wirebond is connected to said capacitor. ~~wherein said one or more wirebonds are connected to said capacitor through said metal line system.~~

7. (currently amended) The ~~integrated~~ circuit component according to claim 1, wherein said power bus comprises gold. ~~discrete capacitor is connected to a post passivation metal line system and wirebonding is also connected to said post passivation metal line system.~~

8. (currently amended) The ~~integrated~~ circuit component according to claim 1 ~~3~~ further comprising:

a passivation layer over said semiconductor substrate,

a contact pad over said passivation layer; and

a wirebond on said contact pad. ~~wherein said discrete capacitor is connected to a post passivation metal line system and to said wirebonds.~~

9. (currently amended) ~~An integrated~~ A circuit component ~~chip~~ comprising:

a semiconductor substrate ~~having semiconductor devices and interconnection lines formed thereover~~;

a transistor in and on said semiconductor substrate;

a first contact pad over said semiconductor substrate;

a passivation layer over ~~overlying~~ said semiconductor substrate, a first opening in said passivation layer exposing a top surface of said first contact pad, wherein said passivation layer comprises nitride; ~~substrate;~~

a second contact pad connected to said top surface, wherein the position of said second contact pad from a top perspective view is different from that of said first contact pad; and

a ~~discrete~~ capacitor ~~mounted above~~ over said passivation layer, wherein said capacitor is connected to said second contact pad. ~~; and~~

~~one or more wirebonds electrically connected to a contact pad formed in openings in said passivation layer.~~

10. (currently amended) The ~~integrated~~ circuit component according to claim 9 further comprising a third contact pad exposed by a second opening in said passivation layer, and a wirebond on said third contact pad. ~~wherein said capacitor connects to a contact pad formed in openings in said passivation layer.~~

11. (currently amended) The ~~integrated~~ circuit component according to claim 9 further comprising a third contact pad over said passivation layer, and a wirebond on said third contact pad. ~~post passivation metal line system overlying said passivation layer.~~

12. (currently amended) The ~~integrated~~ circuit component according to claim 9 ~~11~~ further comprising a third contact pad exposed by a second opening in said passivation layer, a fourth contact pad on said third contact pad, and a wirebond on said fourth contact pad. ~~wherein said discrete capacitor is connected to said post-passivation metal line system and to said wirebonds.~~

13. (currently amended) The ~~integrated~~ circuit component according to claim 9 further comprising a solder connecting said capacitor to said second contact pad. ~~wherein said contact pad comprises an aluminum pad exposed through said openings in said passivation layer.~~

14. (currently amended) The ~~integrated~~ circuit component according to claim 9, wherein said second contact pad comprises gold. ~~wherein said contact pad comprises a metal cap formed in said opening on an aluminum pad.~~

15. (currently amended) ~~An integrated~~ A circuit component comprising:

a semiconductor substrate;

a transistor ~~semiconductor device structures~~ in and on said semiconductor a substrate;

a first metal pad over said semiconductor substrate;

a second metal pad over said semiconductor substrate, wherein said second metal pad is used to be wirebonded thereto;

~~a plurality of levels of interconnection lines and interlevel dielectric materials overlying and connecting said semiconductor device structures wherein there is at least one contact pad connected to said interconnection lines;~~

~~a passivation layer overlying said plurality of levels of interconnection lines and interlevel dielectric materials;~~

~~wirebonds formed overlying said passivation layer and connected to said at least one contact pad; and~~

~~at least one discrete decoupling~~ a capacitor over said semiconductor substrate; and

a solder connecting said capacitor to said first metal pad. ~~mounted on a solder wettable surface over said passivation layer.~~

16. (currently amended) The ~~integrated~~ circuit component according to claim 15 further comprising a wirebond on said second metal pad, wherein said wirebond comprises ~~wirebonds comprise~~ gold.

17. (currently amended) The ~~integrated~~ circuit component according to claim 15 wherein said first metal pad ~~solder wettable surface~~ comprises gold. ~~a printed solder cream.~~

18. (currently amended) The ~~integrated~~ circuit component according to claim 15 wherein said first metal pad ~~solder wettable surface~~ comprises ~~solder,~~ copper~~, or gold~~.

19. (currently amended) The ~~integrated~~ circuit component according to claim 15 further

comprising a ground bus connected to said capacitor. ~~further comprising a diffusion barrier metal layer underlying material having said solder wettable surface.~~

20. (currently amended) The ~~integrated~~ circuit component according to claim ~~15~~16, wherein said ~~at least one decoupling~~ capacitor is connected to said wirebond. ~~wirebonds through said contact pad underlying said passivation layer.~~

21. (currently amended) The ~~integrated~~ circuit component according to claim 15 further comprising a power bus connected to said capacitor. ~~wherein said at least one discrete decoupling capacitor is connected to power/ground buses within said substrate.~~

22. (currently amended) The ~~integrated~~ circuit component according to claim 15 further comprising a first metallization structure over said semiconductor substrate, a passivation layer over said first metallization structure, and a second metallization structure ~~thick metal lines formed overlying~~ over said passivation layer, wherein said second metallization structure is provided with said first metal pad.

23. (currently amended) The ~~integrated~~ circuit component according to claim ~~15~~16 ~~22~~ further comprising a first metallization structure over said semiconductor substrate, a passivation layer over said first metallization structure, and a second metallization structure over said passivation layer, wherein said capacitor is connected to said wirebond through said second metallization structure. ~~thick metal lines are connected to said contact pad through openings in said passivation layer.~~

24. (currently amended) The ~~integrated~~ circuit component according to claim 15 ~~22~~ further comprising a first metallization structure over said semiconductor substrate, a passivation layer over said first metallization structure, and a second metallization structure over said passivation layer, wherein said second metallization structure is provided with said second metal pad. ~~wherein said at least one decoupling capacitor is connected to said wirebonds through said thick metal lines.~~

25. (currently amended) The ~~integrated~~ circuit component according to claim 15 further comprising a passivation layer over said semiconductor substrate, wherein said second metal pad is exposed by an opening in said passivation layer and wherein said passivation layer comprises nitride. ~~solder wettable surface lies on said thick metal lines.~~

26. (currently amended) The ~~integrated~~ circuit component according to claim 15 further comprising a third metal pad over said semiconductor substrate, and a passivation layer over said semiconductor substrate, an opening in said passivation layer exposing said third metal pad, wherein said second metal pad is on said third metal pad and wherein said passivation layer comprises nitride. ~~wirebonds are formed on said contact pad.~~

27. (currently amended) The ~~integrated~~ circuit component according to claim 15, wherein said second metal pad comprises gold. ~~wirebonds are formed on said thick metal lines.~~

28. (currently amended) The ~~integrated~~ circuit component according to claim 15, wherein

said second metal pad comprises aluminum. ~~a gold pad is formed underlying said wirebond.~~

29. (withdrawn ~~and -~~ currently amended) The ~~integrated~~ circuit component according to claim 15 further comprising a first metallization structure over said semiconductor substrate, a passivation layer over said first metallization structure, a polymer layer over said passivation layer, and a second metallization structure over said polymer layer, wherein said second metallization structure is provided with said first metal pad. ~~: a first post-passivation dielectric layer overlying said passivation layer; and thick metal lines formed overlying said first post-passivation dielectric layer and connected to said contact pad through openings in said first post-passivation dielectric layer and said passivation layer wherein said at least one decoupling capacitor is connected to said wirebonds through said thick metal lines.~~

30. (withdrawn and currently amended) The ~~integrated~~ circuit component according to claim 29, wherein said polymer layer ~~first post-passivation dielectric layer~~ comprises polyimide~~, BCB, a porous dielectric material, parylene, or an elastomer~~.

31. (currently amended) The ~~integrated~~ circuit component according to claim 15 ~~29~~ further comprising a first metallization structure over said semiconductor substrate, a passivation layer over said first metallization structure, a second metallization structure over said passivation layer layer, and a polymer layer over said second metallization structure, wherein said second metallization structure is provided with said first metal pad, and an

opening in said polymer layer exposes said first metal pad. ~~a second post-passivation dielectric layer overlying said thick metal lines wherein said at least one decoupling capacitor is connected to said thick metal lines through openings in said second post-passivation dielectric layer.~~

32. (withdrawn ~~and -~~ currently amended) The ~~integrated~~ circuit component according to claim 15 further comprising a first metallization structure over said semiconductor substrate, a passivation layer over said first metallization structure, a polymer layer over said passivation layer, and a second metallization structure over said polymer layer, wherein said second metallization structure is provided with said second metal pad. ~~: first thick metal lines overlying said passivation layer and connected to said contact pad through openings in said passivation layer; a first post-passivation dielectric layer overlying said first thick metal lines; second thick metal lines formed overlying said first post-passivation dielectric layer and connected to said first thick metal lines through openings in said first post-passivation dielectric layer; and a second post-passivation dielectric layer overlying said second thick metal lines wherein said at least one decoupling capacitor is connected to said wirebonds through said second thick metal lines.~~

33. (withdrawn ~~and -~~ currently amended) The ~~integrated~~ circuit component according to claim 32, wherein said polymer layer comprises ~~first and second post-passivation dielectric layers comprise~~ polyimide~~, BCB, a porous dielectric material, parylene, or an~~

~~elastomer~~.

Claims 34-39 (canceled)

40. (currently amended) A method of fabricating ~~an integrated~~ a circuit component ~~chip~~ comprising:

providing a semiconductor substrate, a transistor in and on said semiconductor substrate, a first contact pad over said semiconductor substrate, a passivation layer over said semiconductor substrate, an opening in said passivation layer exposing a top surface of said first contact pad, and a second contact pad connected to said top surface, wherein the position of said second contact pad from a top perspective view is different from that of said first contact pad and wherein said passivation layer comprises nitride; and

~~forming semiconductor device structures in and on a substrate;~~

~~forming a plurality of levels of interconnection lines and interlevel dielectric materials overlying and connecting said semiconductor device structures wherein a topmost level of said interconnection lines includes at least one contact pad;~~

~~depositing a passivation layer overlying said plurality of levels of interconnection lines and interlevel dielectric materials;~~

~~forming first thick metal lines overlying said passivation layer and connecting to said at least one contact pad through openings in said passivation layer;~~

~~forming wirebonds on said first thick metal lines;~~

~~forming a solder wettable surface on said first thick metal lines adjacent to said wirebonds; and~~

mounting ~~at least one discrete decoupling~~ a capacitor over said passivation layer, wherein said capacitor is connected to said second contact pad. ~~on said solder wettable surface.~~

41. (currently amended) The method according to claim 40, wherein forming said second contact pad comprises electroplating. ~~said wirebonds comprise gold.~~

42. (currently amended) The method according to claim 40, wherein forming said second contact pad comprises electroless plating. ~~said step of forming said solder wettable surface comprises printing a solder cream on said thick metal lines.~~

43. (currently amended) The method according to claim 40, wherein forming said second contact pad comprises sputtering. ~~said step of forming said solder wettable surface comprises electroplating, electroless plating, or sputtering said thick metal lines with solder, copper, or gold.~~

44. (currently amended) The method according to claim 40, wherein forming said second contact pad comprises printing. ~~further comprising depositing a diffusion barrier metal layer underlying said solder wettable surface and overlying said thick metal lines.~~

45. (currently amended) The method according to claim 40, wherein said mounting said capacitor comprises using a surface mount technology (SMT). ~~further comprising: depositing a first post passivation dielectric layer overlying said passivation layer and~~

~~underlying said first thick metal lines.~~

46. (withdrawn and currently amended) The method according to claim 40 ~~45~~ further comprising providing a polymer layer over said passivation layer, wherein said second contact pad is on said polymer layer. ~~wherein said first post-passivation dielectric layer comprises polyimide, BCB, a porous dielectric material, parylene, or an elastomer.~~

47. (currently amended) The method according to claim 40 ~~45~~ further comprising providing a polymer layer over said passivation layer, wherein an opening in said polymer layer exposes said second contact pad. ~~depositing a second post-passivation dielectric layer overlying said first thick metal lines.~~

48. (currently amended) The integrated circuit according to claim ~~47~~ 40 further comprising forming a wirebond over said semiconductor substrate. ~~wherein said second post-passivation dielectric layer comprises polyimide, BCB, a porous dielectric material, parylene, or an elastomer.~~

49. (currently amended) The method according to claim 40, wherein forming said second contact pad comprises depositing gold. ~~further comprising: depositing a first post-passivation dielectric layer overlying said first thick metal lines and wherein said wirebonds and said solder pads are formed through openings in said first post-passivation dielectric layer to said first thick metal lines.~~

50. (currently amended) The method according to claim 40, ~~49~~ wherein forming said second contact pad comprises depositing copper. ~~said first post-passivation dielectric layer comprises polyimide, BCB, a porous dielectric material, parylene, or an elastomer.~~

51. (currently amended) The method according to claim 40, wherein forming said second contact pad comprises depositing solder. ~~said at least one discrete decoupling capacitor is connected to wirebonds and to power/ground buses within said substrate.~~

Claims 52-75 (canceled)

76. (new) A method of fabricating a circuit component comprising:

providing a semiconductor substrate, a transistor in and on said semiconductor substrate, a first contact pad over said semiconductor substrate, and a second contact pad over said semiconductor substrate, wherein said second contact pad is used to be wirebonded thereto; and

mounting a capacitor over said semiconductor substrate, wherein said capacitor is connected to said first contact pad.

77. (new) The method according to claim 76, wherein said forming said first contact pad comprises printing.

78. (new) The method according to claim 76, wherein said forming said first contact pad comprises electroplating.

79. (new) The method according to claim 76, wherein said forming said first contact pad comprises electroless plating.

80. (new) The method according to claim 76, wherein said mounting said capacitor comprises using a surface mount technology (SMT).

81. (new) The method according to claim 76 further comprising forming a wirebond connected to said second contact pad.

82. (new) The method according to claim 76, wherein said capacitor is connected to said first contact pad through a solder.

83. (new) A method of fabricating a circuit component comprising:

providing a semiconductor substrate, a transistor in and on said semiconductor substrate, a power bus over said semiconductor substrate, and a ground bus over said semiconductor substrate; and

mounting a capacitor over said semiconductor substrate, wherein said capacitor is connected to said power and ground buses.

84. (new) The method according to claim 83 further comprising providing a contact pad connected to said power bus, wherein forming said contact pad comprises printing.

85. (new) The method according to claim 83 further comprising providing a contact pad connected to said power bus, wherein forming said contact pad comprises electroplating.

86. (new) The method according to claim 83 further comprising providing a contact pad connected to said power bus, wherein forming said contact pad comprises electroless plating.

87. (new) The method according to claim 83, wherein said mounting said capacitor comprises using a surface mount technology (SMT).

88. (new) The method according to claim 83 further comprising forming a wirebond over said semiconductor substrate.

89. (new) The method according to claim 83, wherein said capacitor is connected to said power and ground buses through multiple solder connections.